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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/686.885	10/15/2003	Kunio Satomi	1232-5176	7563

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/686,885	SATOMI ET AL.
	Examiner	Art Unit
	Nitin Parekh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Sawai (US Pat. 6177724).

Regarding claim 1, Sawai discloses an area array semiconductor device/electronic circuit board device (Fig. 3-5) comprising:

- an insulating resin interposer substrate (RIS)/circuit board frame (CBF)/circuit wiring substrate/CWS (2/6 in Fig. 3-5; Col. 4, line 54) having a circuit wiring/connecting lands and a plurality of solder balls (3 in Fig. 1-4) providing internal and external electrical connection
- a semiconductor chip (4 in Fig. 3) having a top face and a bottom face being mounted on the RIS/CBF/CWS and electrically connected with the circuit wiring
- a sealing layer/protective material composed of a sealing resin/resin mold/moldable material (see 1a and 1b in Fig. 1-5) entirely encapsulating the chip, a portion of the top/upper surface of the RIS/CBF/CWS and being positioned on the top face of the chip, the sealing layer/protective material in

conjunction with the RIS/CBF/CWS further providing functions including protection from contamination/moisture in the atmosphere, and

- the sealing layer/resin mold is formed such that the sealing layer/resin mold comprises resin/mold ribs extending in radial directions (see 9 in the resin region 1b in Fig. 5), the resin/mold ribs having an angle of about 45 degree with respect to the sides of the RIS/CBF/CWS to provide improved strength (Col. 5, lines 25-45)

(Fig. 1-5; Col. 4, line 36- Col. 5, line 45).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 3, 5-8 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sawai (US Pat. 6177724) in view of Murayama (US Pat. 6303998).

Regarding claims 2 and 3, Sawai teaches substantially the entire claimed structure as applied to claim 1 above, except the chip having substantially the same angle with respect to the side of the CWS as that of the sealing resin layer with respect to the side of the CWS.

Murayama teaches an area array device having a chip (see 10 and 12 in Fig. 3) wherein:

- the chip is mounted at the angle of about 45 degree with respect a side the CWS (see Fig. 3) to reduce warpage for the device (Col. 4, line 65- Col. 5, line 45), and
- the device being bonded/soldered to solder bumps of an electronic circuit board/printed wiring board (PWB) as a mother board (28 in Fig. 8; Col. 7, lines 10-15).

It would have been obvious to a person of ordinary skill in the art at the time invention was made incorporate the chip having substantially the same angle with respect to the side of the CWS as that of the sealing resin layer with respect to the side of the CWS and the device being soldered to the motherboard as taught by Murayama so that the resin strength can be improved, the stress/warpage can be reduced and the desired external connection can be accomplished in Sawai's device

Regarding claims 5-7, Sawai teaches the entire claimed structure as applied to claim 1 above, wherein Sawai teaches a periphery of the resin not being extended to a of the RIS/CBF/CWS (see 1 and 2 in Fig. 1-4), but Sawai fail to teach the chip having a plurality of sides, each of the sides being at an angle of 30-60 deg. with respect to a corresponding side of the intererposer and the resin having a plurality of sides angled at the same angle with respect to the interposer as the chip.

Murayama teaches an area array device having a chip (see 10 and 12 in Fig. 3) wherein:

- the chip is mounted at the angle of about 45 degree with respect a side the CWS (see Fig. 3) to reduce warpage for the device (Col. 4, line 65- Col. 5, line 45), and
- the device being bonded/soldered to solder bumps of an electronic circuit board/printed wiring board (PWB) as a mother board (28 in Fig. 8; Col. 7, lines 10-15).

It would have been obvious to a person of ordinary skill in the art at the time invention was made incorporate the chip having a plurality of sides, each of the sides being at an angle of 30-60 deg. with respect to a corresponding side of the intererposer and the resin having a plurality of sides angled at the same angle with respect to the interposer as the chip as taught by Murayama so that the resin strength can be improved, the stress/warpage can be reduced and the desired external connection can be accomplished in Sawai's device.

Regarding claims 8, 12 and 13, Sawai and Murayama teach substantially the entire claimed structure as applied to claims 1 and 5 above, wherein the electronic circuit board device comprises the PWB and the sealing resin/protective material.

Regarding claim 14, Sawai teach the entire claimed structure as applied to claim 1 above, except a side of the semiconductor chip being arranged parallel to the side of the circuit wiring substrate.

Murayama teaches a conventional device (see Fig. 1) wherein a chip is arranged parallel to the side of a CWS (see 12 and 10 respectively in Fig. 1; Col. 1).

It would have been obvious to a person of ordinary skill in the art at the time invention was made incorporate the side of the semiconductor chip being arranged parallel to the side of the circuit wiring substrate as taught by Murayama so that the device processing can be simplified in Sawai's device.

5. Claims 4 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sawai (US Pat. 6177724) and Murayama (US Pat. 6303998) as applied to claims 1 3 and 8, and further in view of Gaku et al. (US Pat. 6350952) and admitted prior art (APA).

Regarding claims 4 and 9-11, Sawai and Murayama teach substantially the entire claimed structure as applied to claims 1, 3 and 8 above, except the device being soldered to the PWB using lead-free solder.

Gaku et al. teach using bumps/balls made of conventional lead-free solder (see a in Fig. 1 and 2; Col. 3, line 58; Col. 9, lines 21-58).

The APA teaches using conventional lead-free solder lead-free solder having a melting point greater than 183 deg. C or 220 deg. C and using a conventional resin providing thermal protection/insulation and protection from contamination/moisture for the chip (see specification pp. 1-3).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the device being soldered to the PWB using lead-free solder having the melting point greater than 183 deg. C or 220 deg. C as taught by Gaku et al. and the APA so that the lead exposure can be reduced and the material handling can be simplified in Murayama and Sawai's device.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NITIN PAREKH
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800

NP
03-12-05